Amendments to the Drawings:

The attached sheet of drawings includes a new Fig. 6. The label of the drawings has been amended correspondingly.

Attachments: Replacement Sheets

Annotated Sheets Showing Changes

New Drawing Sheet

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-9 remain in the application. Claim 1 has been amended.

In item 1 on page 2 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims.

More specifically, the Examiner has stated that the method steps:

defining a plurality of subareas...;

using first commands for accessing a first subarea ... and second commands for accessing a second subarea ... to form, ..., a compressed command sequence, ...; and

writing and/or reading the information by executing in all of the memory banks ..., must be shown or the feature(s) cancelled from the claim(s).

Fig. 6 has been added to show the above-mentioned method steps. The specification has been amended accordingly. Also, it is noted that it is clearly shown in Fig. 3 that a

plurality of subareas (A1, A2, A3, A4; B1, ... B4; ..., D4) are defined in each of the memory banks (A, B, C, D).

In item 2 on page 2 of the above-identified Office action, the abstract has been objected to because it repeats information given in the title. Appropriate correction has been made.

In item 4 on page 3 of the above-identified Office action, claims 1-9 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner has stated that claim 1 is a method for testing a semiconductor memory, but there isn't any testing step recited in the body of the claim.

The Examiner's rejection is not understood. The body of claim 1 clearly recites the steps necessary for testing a semiconductor memory, namely each of the memory banks is divided into subareas, a compressed command sequence is formed from first commands and second commands, and a test writing and reading is then performed by executing the respective compressed command sequences. The language of claim 1 has been modified to clearly recite that the writing and reading of the information is for the purpose of testing.

The Examiner has also stated that the language "the testing involving information being written to memory addresses and/or being read from the memory addresses" in lines 2-4 and "...being inserted between the first commands" in lines 15-16 of claim 1 is not clear as what it means.

With regard to the language "the testing involving information being written to memory addresses and/or being read from the memory addresses," it is noted that it is customary to a person skilled in the art that in a functional test of a memory device (see page 16, line 23 of the specification of the instant application), data are testwise written to memory addresses and read out in order to check, by comparison of the read out data with the data written before, whether the data have been stored correctly. Although it is clear to a person skilled in the art that any information testwise written for testing purpose is also read out for checking correct storage operation, this feature has now been recited in amended claim 1 explicitly. Support for the change may be found on page 1, lines 16-20 and page 16, lines 20-25 of the Specification of the instant application.

With regard to the language "...being inserted between the first commands," this limitation means that, in the temporal order of first commands (addressing first subareas (A1; B1;

C1; D1) of the respective memory banks) and second commands (addressing second subareas (A2; B2; C2; D2) of the respective memory banks), the first and second commands are executed alternately. This alternating sequence of first and second commands directly results from the feature that the first commands are associated with the uneven clock periods whereas the second commands are associated with the even clock periods. In order to avoid any possible confusion, the language "...being inserted between the first commands" has been deleted.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved. The above-noted changes to the claims are provided solely for cosmetic and/or clarificatory reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

In view of the foregoing, reconsideration and allowance of claims 1-9, or alternatively issuance of an Office action on the merits are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

/Yonghong Chen/

Yonghong Chen
Reg. No. 56,150

For Applicant

YC

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

1/5

FIG 1 Prior Art

Clock	Command (Bank A)
1	act-A-adr 1
2	0
3	rd-A-adr 1
4	0
5	0
6	0
7	pre-A-adr 1
8	0
9	act-A-adr 2
10	0
11	rd-A-adr 2
12	0
13	0
14	0
15	pre-A-adr 2
16	0

FIG 2 Prior Art

Clock	Command
1	act-A
2	pre-B
3	rd-A
4	act-B
5	pre-C
6	rd-B
7	act-C
8	pre-D
9	rd-C
10	act-D
11	pre-A
12	rd-D

ord={act, pre, rd, wr}

X={A, B, C, D}

Applic. No.: 10/631,356
Amdt. Dated February 2, 2006
Reply to Office action of November 2, 2005
Annotated Sheet Showing Changes

2/5

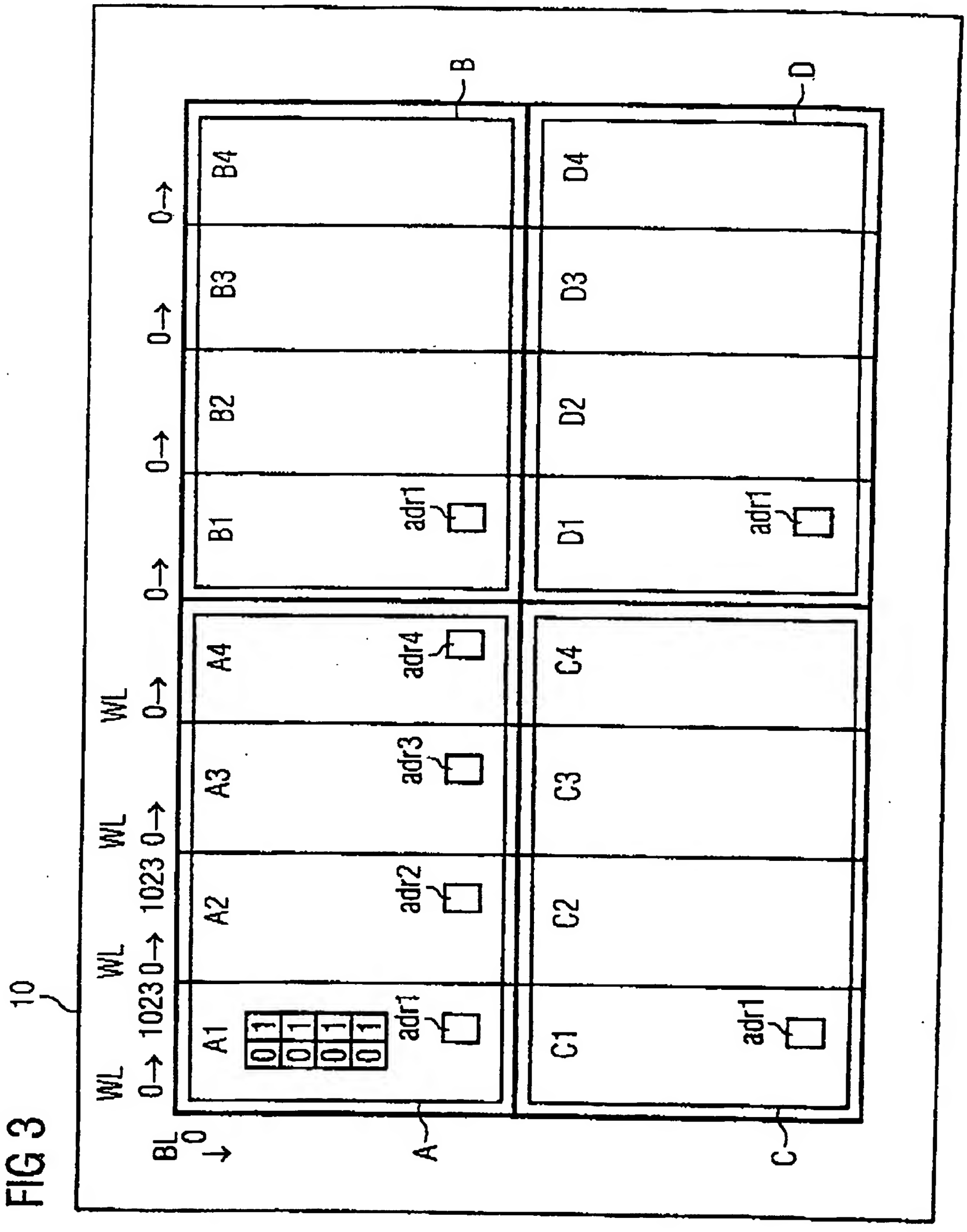


FIG 3

3/5

FIG 4

Command Sequence {ord-Xn-adrN} :

Clock Period	(Bank A)	(Bank B)	(Bank C)	(Bank D)
1	act-A1-adr 1	act-B1-adr 1	act-C1-adr 1	act-D1-adr 1
2	pre-A2-adr 2	pre-B2-adr 2	pre-C2-adr 2	pre-D2-adr 2
3	rd-A1-adr 1	rd-B1-adr 1	rd-C1-adr 1	rd-D1-adr 1
4	act-A2-adr 2	act-B2-adr 2	act-C2-adr 2	act-D2-adr 2
5	pre-A3-adr 3	pre-B3-adr 3	pre-C3-adr 3	pre-D3-adr 3
6	rd-A2-adr 2	rd-B2-adr 2	rd-C2-adr 2	rd-D2-adr 2
7	act-A3-adr 3	act-B3-adr 3	act-C3-adr 3	act-D3-adr 3
8	pre-A4-adr 4	pre-B4-adr 4	pre-C4-adr 4	pre-D4-adr 4
9	rd-A3-adr 3	rd-B3-adr 3	rd-C3-adr 3	rd-D3-adr 3
10	act-A4-adr 4	act-B4-adr 4	act-C4-adr 4	act-D4-adr 4
11	pre-A1-adr 1	pre-B1-adr 1	pre-C1-adr 1	pre-D1-adr 1
12	rd-A4-adr 4	rd-B4-adr 4	rd-C4-adr 4	rd-D4-adr 4
13	act-A1-adr 5	act-B1-adr 5	act-C1-adr 5	act-D1-adr 5
14	pre-A2-adr 6	pre-B2-adr 6	pre-C2-adr 6	pre-D2-adr 6
15	rd-A1-adr 5	rd-B1-adr 5	rd-C1-adr 5	rd-D1-adr 5
16	act-A2-adr 6	act-B2-adr 6	act-C2-adr 6	act-D2-adr 6
17	pre-A3-adr 7	pre-B3-adr 7	pre-C3-adr 7	pre-D3-adr 7
18	rd-A2-adr 6	rd-B2-adr 6	rd-C2-adr 6	rd-D2-adr 6
19	act-A3-adr 7	act-B3-adr 7	act-C3-adr 7	act-D3-adr 7
20	pre-A4-adr 8	pre-B4-adr 8	pre-C4-adr 8	pre-D4-adr 8
21	rd-A3-adr 7	rd-B3-adr 7	rd-C3-adr 7	rd-D3-adr 7
22	act-A4-adr 8	act-B4-adr 8	act-C4-adr 8	act-D4-adr 8
23	pre-A1-adr 5	pre-B1-adr 5	pre-C1-adr 5	pre-D1-adr 5
24	rd-A4-adr 8	rd-B4-adr 8	rd-C4-adr 8	rd-D4-adr 8

12A 12B 12C 12D

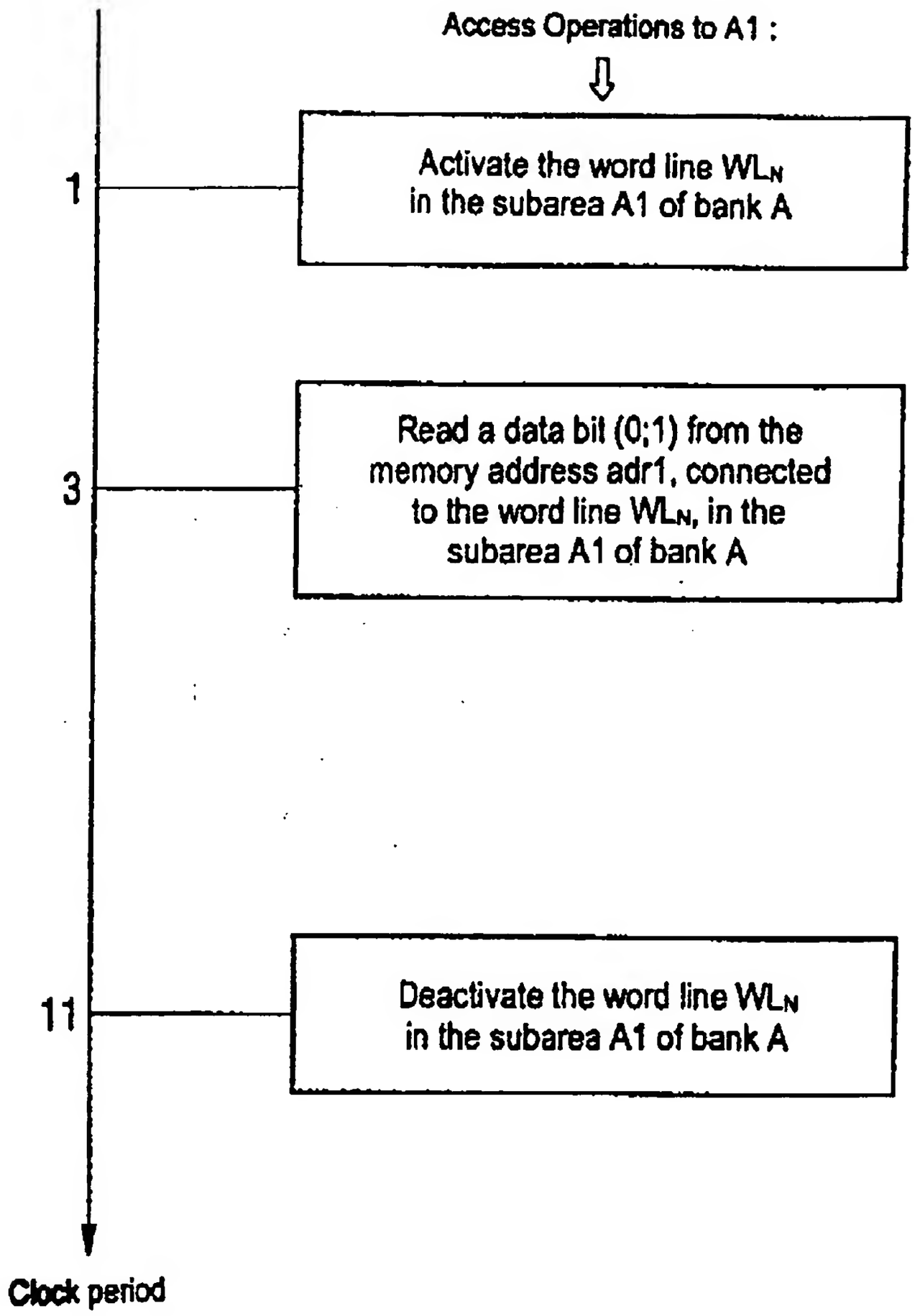
13

14

13A, 14A 13B, 14B 13C, 14C 13D, 14D

4/5

FIG 5


Access Operations to A1 :
1
Activate the word line WLN in the subarea A1 of bank A
3
Read a data bit (0;1) from the memory address adr1, connected to the word line WLN, in the subarea A1 of bank A
11
Deactivate the word line WLN in the subarea A1 of bank A
Clock period